Instructions

- The solutions to all the problems in this homework should be the result of the student’s individual effort. Presenting the words or ideas of somebody else under your name hinders your skills in academic research and violates the university’s policy on academic integrity: http://www.provost.pitt.edu/info/ai1.html
- Turn in a hardcopy of your solutions at the end of the session on **Tuesday February 18th, 2014**.
- Late submissions will not be accepted.

Problem 1

Suppose that a classroom of \( p \) students, each sitting at a desk, is to compute the sum of \( n \) numbers, each of which is written on an index card. In one unit of time a given student can either add two numbers and write the sum on a card, or pass a card to another student at an adjacent desk (i.e., at most an arm’s length away). Assuming that \( n \geq p \), derive an expression for the minimum time to compute the overall sum. Assume a uniform distribution of cards and a square arrangement of desks.

Problem 2

Derive an expression (a reasonably simple function of the number of processors \( p \)) for the average distance (in hops) between any two processors (i.e., the average over all pairs of distinct nodes) in each of the following networks:

(a) 1D-mesh with \( p \) processors.
(b) 1D-torus with \( p \) processors.
(c) 2D-mesh with \( p^2 \) processors.

Problem 3

The XY deterministic routing algorithm shown in lecture *Interconnects* provides an optimal routing on a 2D-mesh without wrap-around links. Using this algorithm as a guide, develop an XYZ deterministic optimal routing algorithm for an 3D-torus (a 3D-mesh with wrap-around links).
Problem 4

Consider a chordal ring network with \( n = 4k \) nodes in which each node \( x, 0 \leq x < n \) is connected with bidirectional links to the four nodes: \( (x + 1) \mod n, (x - 1) \mod n, (x + 4) \mod n \) and \( (x - 4) \mod n \). Find the diameter and the bisection width of this network (for any \( n \)).

Problem 5

Consider the MSI protocol for a bus-based system with three processors \( P_1, P_2 \) and \( P_3 \), each with a direct-mapped cache and assume that the size of a cache line is one word. The following sequence of memory operations access two memory locations (words), \( A \) and \( B \), that are mapped to the same cache location:

\[
\begin{align*}
P_1 & \text{ writes } A = 4 \\
P_3 & \text{ writes } B = 8 \\
P_2 & \text{ reads } A \\
P_3 & \text{ reads } A \\
P_3 & \text{ writes } A = 12 \\
P_2 & \text{ reads } A \\
P_1 & \text{ reads } B \\
P_1 & \text{ writes } B = 10 \\
\end{align*}
\]

Assume that initially, \( A = B = 3 \) and that the cache is initially empty. For each memory access, determine:

(a) The content and state of the cache line in each processor (modified, shared, invalid).
(b) The bus operations caused by the MSI protocol (read request, read data, write back).